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FOLEY AND LARDNER LLP
SUITE 500
3000 K STREET NW
WASHINGTON, DC 20007

EXAMINER	
MOORE, IAN N	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/667,320	SHIMOJO ET AL.	
	Examiner	Art Unit	
	Ian N. Moore	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on 8-21-2007 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of 12/15/1999 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: **USING PRIORITY CONTROL BASED ON CONGESTION STATUS WITHIN PACKET SWITCH**

Claim Objections

3. Claims 1-16 are objected to because of the following informalities:

Claim 1 recites "**a packet**" in line 10. For consistency and clarification with "a packet" recited in line 7, it is suggested to change "a packet" in line 10, to "**the** packet".

Claims 2, 10, 11 and 14 are also objected for the same reason as set forth above in claim 1.

Claim 5 recites "**a** plurality of the input side transfer units" in line 5. For consistency and clarification with "**a** plurality of the input side transfer units" recited in claim 1, line 2, it is suggested to change "**a** plurality of the input side transfer units" in line 5, to "**the** plurality of the input side transfer units".

Claim 10 recites "**those** packets" in line 4. For consistency and clarification, it is suggested to specifically recite what "those" represents (e.g. the plurality of packets).

Claim 11 recites "a packet collision" in line 5. For consistency and clarification with "a packet collision" recited in claim 1, line 14, it is suggested to change "a packet collision" in line 5, to "**the** packet collision".

Claim 12 is also objected for the same reason as set forth above in claim 11.

Claim 12 recites "**a packer**" in line 1. It is suggested to change "a packer" to "**the packet**".

Claim 15 recites "**a packet**" in line 11 and 15. For consistency and clarification with "a packet" recited in line 8, it is suggested to change "the packet" in lines 11 and 15, to "**the** packet".

Claim 17 recites "**a packet**" in line 5. For consistency and clarification with "a packet" recited in line 2, it is suggested to change "a packet" in line 5, to "**the** packet".

Claims 3-4, 6-9, 13, 16 are also objected since they are depended upon objected claims 1 and 15 as set forth above.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 15 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 recites, "a packet collision **may occur**" in line 15 renders the claim indefinite because it is unclear whether a packet collision "occur" or "does not occur".

Claim 16 is also objected since they are depended upon objected claims 15 as set forth above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 5-9 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fan (US005412648A) in view of Hannaka (US005583858A).

Regarding Claim 1, Fan discloses a packet switch (see FIG. 1, ATM self-routing switching system), comprising:

a plurality of input side transfer units (see FIG. 1, a combined system of Line Circuits (LC) 11_N, incoming RIRO buffers 12_N, and input controller 13_N) from which packets are entered (see col. 2, line 50-65, from cells are incoming) ;

a plurality of output side transfer units (see FIG. 1, a combined system of outgoing FIFO buffers CBR_N,VBR_N and output controller 19_N) from which packets are outputted (see col. 2, line 62 to col. 3, line 16; from cells are outgoing);

a switching unit (see FIG. 1, Self routing network 15) through which each packet entered from each input side transfer unit (see FIG. 1, each cell incoming from a combined system of Line Circuits (LC) 11_N, incoming RIRO buffers 12_N, and input controller 13_N) is switched to a desired output side transfer unit (see FIG. 1, is switched to specific outgoing FIFO; see col. 3, line 15-36);

a congestion status monitoring unit (see FIG. 1, a combined system of comparator 31,33 and Idle Space Counter (ISC) 30,32) configured to monitor a congestion status of said one of output side transfer units (see col. 3, line 36-65; see col. 4, line 1-10,21-67, monitor/determine the busy/idle status/state of the outgoing a combined system of outgoing FIFO buffers CBR_N,VBR_N and output controller 19_N) to which a packet from one of said input side transfer units is destined to reach within the packet switch (see FIG. 1, to which a cell from combined incoming a combined system of Line Circuits (LC) 11_N, incoming RIRO buffers 12_N, and input controller 13_N is transmitted/destined to arrive/access/reach to the self routing network 15; see col. 3, line 36-65; see col. 4, line 1-10,21-67);

a priority level attaching unit (see FIG. 1, Input Controller 13_N) configured to process each packet (see col. 2, line 52- to col. 3, line 15; see col. 4, line 10-21; processing each cell), according to the congestion status of one if said output side transfer units (see FIG. 1, according to busy/idle state/status (bits) of $FIFO_N$; see col. 3, line 36-65; see col. 4, line 4-21) to which a packet from one of said input side transfer units is destined to reach which is monitored by the

congestion status monitoring unit (see FIG. 1, to which a cell from combined incoming a combined system of Line Circuits (LC) 11_N, incoming RIRO buffers 12_N, and input controller 13 $_N$ is transmitted/destined to arrive/access/reach the self which is monitored/determined by the combined system of comparator 31,33 and Idle Space Counter (ISC) 30,32; see col. 3, line 36-65; see col. 4, line 4-21); and

a packet selection unit (see FIG. 1, Priority Selector 34) configured to select one packet that is to be transferred at a higher priority (see FIG. 1, selecting CBR cells) among colliding packets when a packet collision occurs (see FIG. 1, among simultaneously-arriving/crashing/colliding VBR and CRB packets), according to the priority level (see col. 3, line 65 to col. 4, line 5; selecting CBR cell first).

Fan does not explicitly disclose "to attach a priority level to each packet" and "within the switching unit", and "attached to each colliding packet".

However, Hannaka teaches a priority level attaching unit (see FIG. 2a-b, 3a-b, Line Handler) configured to attach a priority level to each packet (see FIG. 2a-b, 3a-b, appending routing tag (RT) with Priority Setting (PS) bit); see col. 4, line 45 to col. 5, line 10) to which a packet from one of said input side is destined to reach (see FIG. 2a-b,3a-b, to which a cell from input side is destined to reach/arrive/access; see col. 4, line 45 to col. 5, line 10) and

a packet selection unit (see FIG. 3b; cell selecting means) configured to select one packet that is to be transferred at a higher priority (see FIG. 3b, selecting ATM cell with higher priority PS=1) among colliding packets when a packet collision occurs within the switching unit (see FIG. 3b, among ATM cells with different PS when ATM cell with PS=1 simultaneously-

arriving/crashing/colliding with ATM cell with PS=0), according to the priority level attached to each colliding packet (see FIG. 3a-b, according to PS attached to each ATM cell).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "to attach a priority level to each packet" and "within the switching unit", and "attached to each colliding packet" as taught by Hannaka in the system of Fan, so that it would provide speedy and simple switching of cells, as suggested by Hannaka; see Hannaka col. 1, line 50-60.

Regarding Claim 2, Fan discloses wherein the priority level attaching unit (see FIG. 1, Input Controller 13_N) process a low priority level to a packet (see FIG. 1, process lower priority VBR cell) for which a congestion level of one of said output side transfer units to which a packet from one of said input side transfer units is destined to reach is higher (see FIG. 1, for congestion/loading level of outgoing FIFO buffers VBR_N to which a cell from a combined system of Line Circuits (LC) 11_N, incoming RIRO buffers 12_N, and input controller 13_N is transmitted to reach/arrive/access is higher (i.e. busy), note when the buffer is busy, the congestion is higher).

Fan does not explicitly disclose "attach" a low priority level.

Hannaka also discloses wherein the priority level attaching unit attached a lower priority level to a packet (see FIG. 1, 2a-b, 3a-b, appending low priority PS=0 to a cell) for one of said output side to which a packet from one of said input side (see col. 4, line 45 to col. 5, line 10; transmitted from input side to output side).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "attach" a low priority level to, as taught by Hannaka in the

system of Fan, so that it would provide speedy and simple switching of cells, as suggested by Hannaka; see Hannaka col. 1, line 50-60.

Regarding Claim 3, Fan discloses wherein the priority level attaching unit (see FIG. 1, input controller 13_N) is provided inside each input side transfer unit (see FIG. 1, is inside a combined system of Line Circuits (LC) 11_N, incoming RIRO buffers 12_N, and input controller 13_N; see col. 2, line 50-65). Hannaka also discloses wherein the priority level attaching unit (see FIG. 2a-b,3a-b, Line Handler) is provided inside each input side transfer unit (see FIG. 2a-b,3a-b, is inside the input side of the switch; see col. 4, line 45 to col. 5, line 10).

Regarding Claim 5, Fan discloses the priority level attaching unit sets the priority level to each packet by referring to a congestion level table (see FIG. 1, input controller 13 sets/places the priority level (e.g. CBR, VBR) to each cell according to Idle/busy memory/table 46) that stores a congestion level set to each prescribed one of said output side transfer unit (see FIG. 1, idle/busy memory/table 46 stores idle/busy pair to each outgoing combined system of 19 and 20) according to the congestion status monitored by the congestion status monitoring unit (see FIG. 1, according to the idle/busy state/status determined/monitored by a combined system of comparator 31,33 and ISC 30,32), the congestion level table being provided for each one or a plurality of the input side transfer units (see FIG. 1, memory 46 is provided for each incoming combined system of input controller 13 and RIFO 12); See col. 3, line 1 to col. 4, line 67.

Fan does not explicitly disclose "to be attached".

However, Hannaka teaches a priority level attaching unit (see FIG. 2a-b,3a-b, Line Handler) sets a priority level to be attached to each packet (see FIG. 2a-b,3a-b, appending routing tag (RT) with Priority Setting (PS) bit); see col. 4, line 45 to col. 5, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "to be attached", as taught by Hannaka in the system of Fan, so that it would provide speedy and simple switching of cells, as suggested by Hannaka; see Hannaka col. 1, line 50-60.

Regarding Claim 6, Fan discloses wherein the congestion status monitoring unit (see FIG. 1, a combined system of comparator 31, 33 and Idle Space Counter (ISC) 30, 32) is provided inside each output side transfer unit (see FIG. 1, inside/part of a combined system of outgoing FIFO buffers CBR_N, VBR_N and output controller 19_N; see col. 2, line 62 to col. 3, line 16).

Regarding Claim 7, Fan discloses the congestion status monitoring unit (see FIG. 1, a combined system of comparator 31, 33 and Idle Space Counter (ISC) 30, 32) monitors the congestion status of

each prescribed one of said output side transfer units (see FIG. 1, a combined system of outgoing FIFO buffers CBR_1, VBR_1 and output controller 19_1) for a corresponding output side transfer unit (see FIG. 1, for a corresponding a combined system of outgoing FIFO buffers CBR_2, VBR_2 and output controller 19_2 ; see col. 2, line 62 to col. 3, line 16); **or**

each class of the corresponding output side transfer unit (see FIG. 1, each CBR_2,VBR_2 class of the corresponding a combined system of outgoing FIFO buffers CBR_2,VBR_2 and output controller 19_2 ; see col. 2, line 62 to col. 3, line 16).

Regarding Claim 8, Fan discloses the congestion status monitoring unit (see FIG. 1, a combined system of comparator 31,33 and Idle Space Counter (ISC) 30,32) notifies a monitored congestion status (see FIG. 1, transmits/notifies busy/idle state/status) such that the monitored

congestion status is reflected into the priority level processed by the priority level attaching unit (see FIG. 1, so that busy/idle state/status is corresponded/reflected/used into CBR,VBR priority levels processed by the input controller 13; see col. 3, line 36-65; see col. 4, line 1-10,21-67).

Fan does not explicitly disclose "attached by".

However, Hannaka teaches a priority level is attached by a priority level attaching unit (see FIG. 2a-b,3a-b, Line Handler; see FIG. 2a-b,3a-b, appending routing tag (RT) with Priority Setting (PS) bit); see col. 4, line 45 to col. 5, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "attached by", as taught by Hannaka in the system of Fan, so that it would provide speedy and simple switching of cells, as suggested by Hannaka; see Hannaka col. 1, line 50-60.

Regarding Claim 9, Fan discloses wherein the priority level attaching unit is provided inside each input side transfer unit (see FIG. 1, input controller 13_N is inside a combined system of Line Circuits (LC) 11_N, incoming RIRO buffers 12_N, and input controller 13_N; see col. 2, line 50-65), and the congestion status monitoring unit (see FIG. 1, a combined system of comparator 31,33 and Idle Space Counter (ISC) 30,32) notifies a prescribed information regarding the monitored congestion status (see FIG. 1, transmits/notifies busy/idle state/status) to one input side transfer unit that has transmitted one packet (see FIG. 1, to the incoming combined system of input controller 13 and RIRO 12 that transmitted one cell; not that RIRO transmits cells to FIFO), at a timing of arrival of said one packet to the output side transfer unit (see FIG. 1, at the time of receiving the cell at FIFO of a combined outgoing system of output controller 19 and FIFO; note that the busy/idle information is only transmitted upon receiving a cell from input

RIRO; see col. 3, line 15 to col. 4, line 67). Hannaka also discloses wherein the priority level attaching unit (see FIG. 2a-b,3a-b, Line Handler) is provided inside each input side transfer unit (see FIG. 2a-b,3a-b, is inside the input side of the switch; see col. 4, line 45 to col. 5, line 10).

Regarding Claim 17, Fan discloses a packet switching method of a packet switch (see FIG. 1, ATM self-routing switching system processing the method FIG. 3) in which a packet is transferred from an input side transfer unit (see FIG. 1, cell is transmitted from a combined system of Line Circuits (LC) 11_N, incoming RIRO buffers 12_N, and input controller 13_N; see col. 2, line 50-65) via a switching unit (see FIG. 1, Self routing network 15; see col. 3, line 15-36) to a desired output side transfer unit (see FIG. 1, to a combined system of outgoing FIFO buffers CBR_N -VBR_N and Output controller 19_N; see col. 2, line 62 to col. 3, line 16), the method comprising:

transferring the packet according to a congestion status of a one of said output side transfer units (see FIG. 1, Input Controller 13_N transmitting the cell according to busy/idle state/status (bits) of target/destination $FIFO_N$; see col. 3, line 36-65; see col. 4, line 4-21) to which a packet from one of said input side transfer unit is destined to reach (see FIG. 1, to which a cell from combined incoming a combined system of Line Circuits (LC) 11_N, incoming RIRO buffers 12_N, and input controller 13_N is transmitted/destined to arrive/access/reach; see col. 3, line 36-65; see col. 4, line 4-21);

switching the packet transferred from the input side transfer unit according to one of said input side transfer units of the packet at the switching unit (see FIG. 1, Self routing network 15 switches the cells transmitted from a combined system of Line Circuits (LC) 11_N, incoming RIRO buffers 12_N, and input controller 13_N; see col. 3, line 15-36), and transferring one

colliding packet selected from colliding packets by accounting for the priority level of each colliding packet (see FIG. 1, transmitting CBR cell from CBR and VBR cells according to priority of each cell), at higher priority to the output side transfer unit when a packet collision occurs (see FIG. 1,transmitting high priority CBR cells to FIFO when arriving/crashing/colliding VBR and CRB packets; see col. 3, line 65 to col. 4, line 5); and

notifying information indicating a monitoring result of the congestion status for a prescribed unit of monitoring (see FIG. 1, a combined system of comparator 31, 33 and Idle Space Counter (ISC) 30, 32 determines/monitors the results of congestion state/status (i.e. busy/idle bits) of the outgoing $FIFO_N$, and transmits/notify busy/idle bits), from the output side transfer unit to which the packet has reached (see FIG. 1, from a combined system of outgoing FIFO buffers CBR_N -VBR_N and Output controller 19_N; see col. 2, line 62 to col. 3, line 16 to which cell is arrived/reach/access) to the input side transfer unit which transmitted the packet (see FIG. 1, to the combined system of Line Circuits (LC) 11_N , incoming RIRO buffers 12_N, and input controller 13_N which transmitted the cell; see col. 4, line 1-10,21-67).

Fan does not explicitly disclose "attaching a priority level" and "within the switching unit".

However, Hannaka teaches attaching a priority level to each packet (see FIG. 2a-b,3a-b, appending routing tag (RT) with Priority Setting (PS) bit); see col. 4, line 45 to col. 5, line 10) to which a packet from one of said input side is destined to reach (see FIG. 2a-b,3a-b, to which a cell from input side is destined to reach/arrive/access; see col. 4, line 45 to col. 5, line 10) and

selecting one packet that is to be transferred at a higher priority (see FIG. 3b, selecting ATM cell with higher priority PS=1) among colliding packets when a packet collision occurs

within the switching unit (see FIG. 3b, among ATM cells with different PS when ATM cell with PS=1 simultaneously-arriving/crashing/colliding with ATM cell with PS=0), according to the priority level attached to each colliding packet (see FIG. 3a-b, according to PS attached to each ATM cell).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide attaching a priority level" and "within the switching unit" as taught by Hannaka in the system of Fan, so that it would provide speedy and simple switching of cells, as suggested by Hannaka; see Hannaka col. 1, line 50-60.

Regarding Claim 18, Fan discloses a computer usable medium storing a computer readable program for causing one or a plurality of computers to function as a packet switch (see FIG. 1, memories/FIFO/RIRO 13,12,20 for causing controllers/computers 13,19 to function as ATM self-routing switching system) in which a packet is transferred from an input side transfer unit (see FIG. 1, cell is transmitted from a combined system of Line Circuits (LC) 11_N, incoming RIRO buffers 12_N, and input controller 13_N; see col. 2, line 50-65) via a switching unit (see FIG. 1, Self routing network 15; see col. 3, line 15-36) to a desired output side transfer unit (see FIG. 1, to a combined system of outgoing FIFO buffers CBR_N -VBR_N and Output controller 19_N; see col. 2, line 62 to col. 3, line 16), the switching unit having a function of processing a priority level that is to be transferred (see FIG. 1, transmitting CBR cell from CBR and VBR cells according to priority of each cell) at a higher priority among colliding packets when a packet collision occurs (see FIG. 1,transmitting high priority CBR cells to FIFO when arriving/crashing/colliding VBR and CRB packets; see col. 3, line 65 to col. 4, line 5), the computer program comprising:

a first computer readable program code for causing said one or a plurality of computers (see FIG. 1, methods/steps/program for causing/processing a combined system of comparator 31,33 and Idle Space Counter (ISC) 30,32) to monitor a congestion status of one of said outside transfer units (see col. 3, line 36-65; see col. 4, line 1-10,21-67, monitor/determine the busy/idle status/state of the outgoing $FIFO_N$) to which a packet from one of said input side transfer units is destined to reach within the packet switch (see FIG. 1, to which a cell from combined incoming $LC\text{-}RIRO_N$ is transmitted/destined to arrive/access/reach to the self routing network 15; see col. 3, line 36-65; see col. 4, line 1-10,21-67);

a second computer readable program code for causing said one or a plurality of computers (see FIG. 1, methods/steps/program for causing/processing Input Controller 13_N) to process each packet (see col. 2, line 52- to col. 3, line 15; see col. 4, line 10-21; processing each cell), according to the congestion status of said output side transfer units (see FIG. 1, according to busy/idle state/status (bits) of $FIFO_N$; see col. 3, line 36-65; see col. 4, line 4-21) which is monitored by the first computer readable program code (see FIG. 1, to which a cell from combined incoming $LC\text{-}RIRO_N$ is transmitted/destined to arrive/access/reach the self which is monitored/determined by the combined system of comparator 31,33 and Idle Space Counter (ISC) 30,32; see col. 3, line 36-65; see col. 4, line 4-21).

Fan does not explicitly disclose "to attach a priority level to each packet" and "within the switching unit", and "attached to each colliding packet".

However, Hannaka teaches a second computer readable program code for causing said one or a plurality of computers (see FIG. 2a-b,3a-b, Line Handler) configured to attach a priority level to each packet (see FIG. 2a-b,3a-b, appending routing tag (RT) with Priority Setting (PS)

bit); see col. 4, line 45 to col. 5, line 10) to which a packet from one of said input side is destined to reach (see FIG. 2a-b,3a-b, to which a cell from input side is destined to reach/arrive/access; see col. 4, line 45 to col. 5, line 10) and

the switch unit (see FIG. 3b; Switch Element) having a function of selecting a priority level packet that is to be transferred at a higher priority (see FIG. 3b, selecting ATM cell with higher priority PS=1) among colliding packets when a packet collision occurs within the switching unit (see FIG. 3b, among ATM cells with different PS when ATM cell with PS=1 simultaneously-arriving/crashing/colliding with ATM cell with PS=0), according to the priority level attached to each colliding packet (see FIG. 3a-b, according to PS attached to each ATM cell).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "to attach a priority level to each packet" and "within the switching unit", and "attached to each colliding packet" as taught by Hannaka in the system of Fan, so that it would provide speedy and simple switching of cells, as suggested by Hannaka; see Hannaka col. 1, line 50-60.

1. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fan and Hannaka as applied to claim 1 above, and further in view of Guthric (US005905877A).

Regarding Claim 4, the combined system of Fan and Hannaka discloses wherein the priority level attaching unit sets (see Fan FIG. 1, Input controller 13; see Hannaka FIG. 2b, Line Hander Li) a high priority level to one or a plurality of packets that are to be transferred to one transfer to one of said output side transfer units initially (see Fan FIG. 1, sets to CBR (high

priority) to a cell that is transmitted to a outgoing combined system of output controller 19 and FIFO; see Fan col. 3, line 36-65; see col. 4, line 4-21; see Hannaka FIG. 2b-3b, set to PR=1 (high priority) to a call that is transmitted to output side) when the congestion status of said one of said output side transfer units that is referred (see Fan FIG. 1, when a busy/idle state/statue of a combined outgoing system that is referred) in order to attach the priority level to each packet (see Hannaka FIG. 2a-b,3a-b, in order to attached PR label to each packet); see Hannaka col. 4, line 45 to col. 5, line 10).

Neither Fan nor Hannaka explicitly discloses "temporarily" and "unknown or invalid".

However, Guthric discloses setting a temporarily high priority level when status is unknown or invalid (see col. 8, line 50-60; see col. 9, line 5-15; dynamic priority is assigned as temporary high priority when status is ingnore/unknown/invlaid).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "temporarily" and "unknown or invalid" as taught by Guthric, in the combined system of Fan and Hannaka, so that it would provide faire and consistent fashion of assigning priority as suggested by Guthric; see Guthric col. 3, line 55-65.

2. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fan and Hannaka as applied to claim 1 above, and further in view of Fan'165 (US006324165B1).

Regarding Claim 10, Fan discloses providing for each input side transfer unit and configured to control an order of transfers of a plurality of packets that are waiting for transfers to the switching unit at each input side transfer unit (see FIG. 1, a combined system of input controller 13 and RIRO 12 controls the arrangement/order of transmission of cells that are

waiting/queuing at each combined incoming system of input controller 13, RIRO 12 and LC 11; see col. 2 , line 65 to col. 3, line 36) such that those packets destined to non-congested one of said output side transfer units are transferred to the switching unit at higher priority by accounting for the congestion status of one of said output side transfer units to which a packet from one of said input side transfer unit is destined to reach (see FIG. 1, so that cells transmitted/destined to idle FIFO of a combined outgoing system of controller 19 and FIFO are transferred/forwarded to self-routing network 15 at CBR (high priority) according to the busy/idle status/state of one the combined outgoing system controller 19 and FIFO to which a cell from the combined incoming system of input controller 13 and RIRO 12 is destined/transmitted to reach/arrive; see col. 3, line 36 to col. 4, line 35).

Neither Fan nor Hannaka explicitly discloses "a scheduling unit provided for each input side transfer unit".

However, Fan'165 discloses a scheduling unit (see FIG. 3, Input module Scheduler) provided for each input side transfer unit (see FIG. 3, in each input module OP1-OP16) and configured to control an order of transfers of a plurality of packets that are waiting for transfers (see FIG. 3, schedule/control the order of transmission of cells that are queuing/waiting for transfers) to the switching unit at each input side transfer unit (see FIG. 3, to the core switch module 34 at each input module 30); see col. 6, line 26 to col. 7, line 9, 25 to col. 8, line 67, such that those packets destined to non-congested one of said output side transfer units are transferred to the switching unit at higher priority (see FIG. 3, so that the cells destined/intended to non-blocked/non-congested (per Table 1) are transmitted to core switch module 34 at real-time higher priority) by accounting for the congestion status of one of said output side transfer

units to which a packet from one of said input side transfer unit is destined to reach (see FIG. 3, according to feedback control signal for congestion/overflow status/state of output module 31 to which a cell from input module 30 is destined/intended to reach/arrive); see col. 7, line 25 to col. 8, line 67).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to "a scheduling unit provided for each input side transfer unit" as taught by Fan'165, in the combined system of Fan and Hannaka, so that it would provide large capacity and ability to provide QoS support for multiple class of traffic, as suggested by Fan'165; see Fan'165 col. 3, line 5-15.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fan and Hannaka as applied to claim 1 above, and further in view of Greene (US005930256A).

Regarding Claim 11, the combined system of Fan and Hannaka discloses wherein a packet (see Fan FIG. 1, cell; see Hannaka FIG. 2a-b,3a-b, cell) with the priority level attached thereto (see Hannaka FIG. 2a-b,3a-b, PS is appended to a cell) is transferred from a input side transfer unit (see Fan FIG. 1, transmitted from a combined incoming system of input controller 13, LC 11 and RIRO 12; see Hannaka FIG. 2b,3b, transmitted from input side) via the switching unit (see Fan FIG. 1, via self routing network 15; see Hannaka FIG. 2b,3b, via switching element) to a output side transfer unit (see Fan FIG. 1, to a combined outgoing system of output controller 19 and FIFO; see Hannaka FIG. 2b,3b, to output side); see Fan col. 3, line 5-65; see Hannaka col. 4, line 45 to col. 5, line 12);

the switching unit transfers one colliding packet selected from colliding packets (see Fan FIG. 1, self routing network 15 transmits one cell; see Hannaka FIG. 2b,3b, switching element transmits one cell arrive at the same time (i.e. colliding cell)) by accounting for the priority level attached to each colliding packet (see Hannaka FIG. 2a-b,3a-b, according to the PS level appended to the cell), to the output side transfer unit when a packet collision occurs inside the switching unit (see Fan FIG. 1, to the outgoing combined system of output controller 19 and FIFO 20; see Hannaka FIG. 2b-3b, to output side when cells arrive at the same time (i.e. packet collision occurs) inside the switch element) while discarding other colliding packets inside the switching unit (see Hannaka FIG. 2b-2c, 7c, 8, discarding lower priority PS, upon arriving cells at the same time, inside the switch element); see Fan col. 3, line 5-65; see Hannaka col. 4, line 60 to col. 5, line 40),

the priority level attaching unit is provided at the input side transfer unit and sets the priority level to be attached to each packet (see Hannaka FIG. 2a-b,3a-b, appending routing tag (RT) with Priority Setting (PS) bit); see Hannaka col. 4, line 45 to col. 5, line 10).

Neither Fan nor Hannaka explicitly discloses "re-transmission packet higher than the priority level originally attached to a corresponding discarded packet".

However, Greene discloses the input side transfer unit re-transmits each discarded packet when a packet discarding due to the packet collision is detected (see col. 7, line 25 to col. 8, line 35, abstract; input side retransmitted the packet when a packet was dropped/discarded due to detecting/determining of unsuccessful transmission), and

sets the priority level to be attached to each re-transmission packet higher than the priority level originally attached to a corresponding discarded packet (col. 7, line 25 to col. 8,

line 35, abstract; increasing priority level attached/appended to the retransmitted packet (i.e. from low to high) compares to original/dropped packet).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to re-transmission packet higher than the priority level originally attached to a corresponding discarded packet" as taught by Greene, in the combined system of Fan and Hannaka, so that it would provide unified architecture that is readily scaleable and simple and advantageously make the switching fabric economical to manufacture as suggested by Greene; see Greene col. 2, line 20-35.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fan and Hannaka as applied to claim 1 above, and further in view of Cash (US005481312A).

Regarding Claim 12, the combined system of Fan and Hannaka discloses wherein a packet (see Fan FIG. 1, cell; see Hannaka FIG. 2a-b,3a-b, cell) with the priority level attached thereto (see Hannaka FIG. 2a-b,3a-b, PS is appended to a cell) is transferred from a input side transfer unit (see Fan FIG. 1, transmitted from a combined incoming system of input controller 13, LC 11 and RIRO 12; see Hannaka FIG. 2b,3b, transmitted from input side) via the switching unit (see Fan FIG. 1, via self routing network 15; see Hannaka FIG. 2b,3b, via switching element) to a output side transfer unit (see Fan FIG. 1, to a combined outgoing system of output controller 19 and FIFO; see Hannaka FIG. 2b,3b, to output side); see Fan col. 3, line 5-65; see Hannaka col. 4, line 45 to col. 5, line 12);

the switching unit transfers one colliding packet selected from colliding packets (see Fan FIG. 1, self routing network 15 transmits one cell; see Hannaka FIG. 2b,3b, switching element

transmits one cell arrive at the same time (i.e. colliding cell)) by accounting for the priority level attached to each colliding packet (see Hannaka FIG. 2a-b,3a-b, according to the PS level appended to the cell), at higher priority to the output side transfer unit when a packet collision occurs inside the switching unit (see Fan FIG. 1, at high priority CBR to the outgoing combined system of output controller 19 and FIFO 20 when both cells arrive simultaneously; see Hannaka FIG. 2b-3b, at high priority state PS to output side when cells arrive at the same time (i.e. packet collision occurs) inside the switch element; see Hannaka col. 4, line 60 to col. 5, line 25);

the priority level attaching unit (see Fan FIG. 1, input controller 13_N) is provided at the input side transfer unit (see Fan FIG. 1, is inside a combined system of Line Circuits (LC) 11_N, incoming RIRO buffers 12_N, and input controller 13_N; see Fan col. 2, line 50-65), and

when a plurality of packets are to be transferred from the input side transfer unit (see Fan FIG. 1, cells are transmitted from a incoming combined system of input controller 13, RIRO 12 and LIC 11; see Hannaka FIG. 2b, 3b, cells are transmitted from input side), the priority level attaching unit sets the priority level of one packet corresponding to a top portion lower than the priority level of other packets corresponding to subsequent packets (see Hannaka FIG. 2b, line hander appends the Priority state PS to top portion of a cell (PS=0), lower than priority state PS of other cell corresponding to subsequence cells; see Hannaka col. 4, line 60 to col. 5, line 25).

Neither Fan nor Hannaka explicitly discloses "constituting one datagram" and "of said one datagram".

However, Cash discloses when a plurality of packets (see FIG. 3, HPn and LPn segments 310) constituting one datagram (see FIG. 3, within/constitute one frame) are to be transferred from the input side transfer unit (see FIG. 2, transmits from input side of server 200/client 230),

setting the priority level of one packet (see FIG. 3, setting/assigning a priority to a segment) corresponding to a top portion of said one datagram (see FIG. 3, correspond to a top/peak/best segment (i.e. LPn)) lower than the priority level of other packets corresponding to subsequent portions of said one datagram (see FIG. 3, lower than priority level of other segments corresponding to the following/successive segments of a frame); see col. 3, line 1-7,43-65, see col. 4, line 30-61).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "constituting one datagram" and "of said one datagram" as taught by Cash, in the combined system of Fan and Hannaka, so that it would provide quality of transmission over packet networks as suggested by Cash; see Cash col. 1, line 30-35.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fan and Hannaka as applied to claim 1 above, and further in view of Wallner (US006442172B1).

Regarding Claim 14, Fan discloses wherein each input side transfer unit (see FIG. 1, a incoming combined system of input controller 13, RIRO 12 and LC 11) transfers a packet from the input side transfer unit at a time of transferring the packet via the switching unit to an output side transfer unit (see FIG. 1, transmitting cell from the combined system of input controller 13, RIRO 12 and LC 11 at a time of transmitting the cell via the switching network to an outgoing combined system of output controller 12 and FIFO; see col. 3, line 3 to col. 3, line 65), and

the output side transfer unit (see FIG. 1, an outgoing combined system of output controller 19 and FIFO) carries out a congestion control in order to control an amount of packet flows flowing through a network in which the packet switch is provided (see FIG. 2b-3b; see col.

3, line 5-65; performs the congestion control by queuing/FIFO-ing the amount of cells flowing through a ATM switching network in which cell switching system is provide; see col. 4, line 5-67).

Fan does not explicitly disclose "along with the congestion status inside".

However, Hannaka discloses wherein each input side transfer unit (see FIG. 2b-3b, input Line Handler Li) transfers a packet along with the congestion status inside the input side transfer unit at a time of transferring the packet (see FIG. 2a-3a, transmits a cell with congestion control information in the routing tag inside the input Line Handler) via the switching unit (see FIG. 2b-3b, switching element) to an output side transfer unit (see FIG. 2b-3b, to output Line handler Li'); see col. 1, line 56-60; see col. 2, line 14-16; see col. 4, line 50-59).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "along with the congestion status inside" , as taught by Hannaka in the system of Fan, so that it would provide speedy and simple switching of cells, as suggested by Hannaka; see Hannaka col. 1, line 50-60.

Neither Fan nor Hannaka explicitly discloses, "the output side transfer unit obtains a comprehensive congestion status using the congestion status inside the input side transfer unit that is notified along with the packet and the congestion status inside the output side transfer unit, and" "using the comprehensive congestion status".

However, Wallner discloses each input side transfer unit (see FIG. 3, source input-output processors (IOP) 310) transfers a packet along with the congestion status inside the input side transfer unit at a time of transferring the packet (see FIG. 3, transmits a content status message with "empty" or "non empty" status inside the IOP 310 at a time of transmitting the message) via

the switching unit (see FIG. 3, switch fabric 300) to an output side transfer unit (see FIG. 3, to destination IOP 320); see col. 4, line 63 to col. 5, line 20;

the output side transfer unit (see FIG. 3, destination IOP 320) obtains a comprehensive congestion status (see FIG. 3, consolidate/comprehensive "empty" or "not empty" status at both IOP 320 and IOP 310) using the congestion status inside the input side transfer unit that is notified along with the packet (see FIG. 3, using the "empty/not empty" status transmitted by the IOP 310; see col. 4, line 65 to col. 5, line 20) and the congestion status inside the output side transfer unit (see FIG. 3, empty/not empty" status at IOP 320 determined by output data flow control unit 326 within; see col. 5, line 20-43, 65 to col. 6, line 30), and carries out a congestion control using the comprehensive congestion status in order to control an amount of packet flows flowing (see FIG. 3, performing flow/congestion control using the consolidate/comprehensive "empty" or "not empty" status at both IOP 320 and IOP 310 in order to control the amount/bandwidth/rate of messages flow; see col. 5, line 1-42; see col. 7, line 29-30; see col. 8, line 14-19; see col. 9, line 42-53) through a network in which the packet switch is provided (see FIG. 2-3, a network that couples to the data switch; see col.4, line 20-36,62-67).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "the output side transfer unit obtains a comprehensive congestion status using the congestion status inside the input side transfer unit that is notified along with the packet and the congestion status inside the output side transfer unit, and" "using the comprehensive congestion status" as taught by Wallner, in the combined system of Fan and Hannaka, so that it would avoid the side effects of handshaking through the expedient of queue status-based buffer control; see Wallner col. 2, line 40-67.

Allowable Subject Matter

6. **Claim 13** is objected to as set forth in paragraph 3 and being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. **Claim 15** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, and objection set forth in paragraph 3 set forth in this Office action.

8. **Claim 16** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and objection set forth in paragraph 3.

Response to Arguments

9. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on 571-272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ian N. Moore
Examiner
Art Unit 2616

11-30-07

DORIS H. TO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600